REMARKS

In the Office Action, the Examiner rejected claims 28-37 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15-23 of United States Patent 6,687,893 B2. The Examiner objected to claims 41 and 43 for informalities. The Examiner rejected claims 36-37 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner rejected claims 38-45 under 35 U.S.C. §102(b) as being anticipated by United States Patent 5,822,214 to Rostoker, et al. (Rostoker). The Examiner also rejected claims 38-43 under 35 U.S.C. §102(e) as being anticipated by United States Patent 6,327,694 B1 to Kanazawa, et al. (Kanazawa). In this Amendment, Applicants have amended claims 36, 38, 41 and 43, but have not added or amended any other claim. Accordingly, claims 28-45 will be pending in the application after entry of this Amendment.

I. Statement of Substance of the Interview

Applicants respectfully thank the Examiner for the personal interview on August 12, 2004. During the personal interview, no exhibit was shown or demonstration conducted. The Applicants' representative discussed claims 38 and 42 with the Examiner. Furthermore, the Applicants' representative discussed Rostoker and Kanazawa with the Examiner.

II. Obviousness-type double patenting

The Examiner rejected claims 28-37 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 15-23 of United States Patent 6,687,893 B2. The Examiner stated that Applicants or their attorney may execute a terminal disclaimer to overcome this objection. Applicants attach a terminal disclaimer executed by their attorney of

record in this matter. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the obviousness-type double patenting rejection of claims 28-37.

III. Objection to claims 41 and 43

The Examiner objected to claims 41 and 43 for an informality. Applicants have amended claims 41 and 43 to correct the informality. According, Applicants respectfully request reconsideration and withdrawal of the objection to claims 41 and 43.

IV. Rejection of claims 36 and 37 under §112, second paragraph

The Examiner rejected claims under §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. Specifically, the Examiner rejected claims 36 and 37 due to lack of antecedent basis for "the first attribute," as recited in claim 36. The Examiner rejected claim 37 based on its dependence on claim 36. Applicants have amended claim 36 to correct the informality. Accordingly, Applicants respectfully request reconsideration and withdrawal of the §112 rejection of claims 36 and 37.

V. Rejection of claims 38-41 under §102(b)

The Examiner rejected claims 38-41 under §102(b) as being anticipated by Rostoker. Claims 39-41 are dependent on claim 38. Claim 38 recites a method that places circuit modules in a region of an integrated circuit ("IC") layout. The IC layout has several circuit elements. Several nets represent interconnections between the circuit elements. Each net is defined to include a set of circuit elements. The method selects a first wiring model from a set of at least two wiring models. Each wiring model provides a wiring direction for each layer of the IC layout. The first wiring model includes a wiring direction that is not available on any layer of at least one other wiring model in the set of wiring models. The method partitions the IC region into several sub-regions. The method selects a net and identifies the set of sub-regions containing the circuit

elements of the selected net. The method retrieves, from a storage structure, a pre-computed attribute of a set of one or more interconnect lines that are necessary for connecting the identified set of sub-regions. The set of interconnect lines are based on the first wiring model.

Applicants respectfully submit that Rostoker does not disclose, teach, or even suggest such a method. For instance, the Office Action cites column 58, line 36 to column 59, line 63, of Rostoker in support of the proposition that Rostoker discloses a method comprising selecting a first wiring model from among a plurality of wiring models, where each model specifying different types of interconnect lines. This portion of Rostoker describes an algorithm to reduce multi-pin nets into pairs of pins. However, this portion of Rostoker does not disclose selecting a first wiring model from a set of at least two wiring models, wherein each wiring model provides a wiring direction for each layer of the IC layout. Moreover, none of the portions cited in Rostoker disclose, teach, or even suggest that the first wiring model includes a wiring direction that is not available on any layer of at least one other wiring model in the set of wiring models. Thus, Applicants respectfully submit that Rostoker does not disclose, teach, or even suggest several limitations of claim 38.

Accordingly, Applicants respectfully submit that Rostoker neither anticipates, nor otherwise invalidates claim 38. Since claims 39-41 are dependent on claim 38, Applicants respectfully submit that Rostoker neither anticipates, nor otherwise invalidates, claims 39-41 for at least the reasons discussed above in relation to claim 38.

In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(b) rejection of claims 38-41.

VI. Rejection of claims 42-45 under §102(b)

The Examiner rejected claims 42-45 under §102(b) as being anticipated by Rostoker. Claims 43-45 are dependent on claim 42. Claim 42 recites a method that places circuit modules in a region of an integrated circuit ("IC") layout. The IC layout has several circuit elements. Several nets represent interconnections between the circuit elements. Each net is defined to include a set of circuit elements. The method selects a first wiring model from a set of at least two wiring models. Each wiring model provides a wiring direction for each layer of the IC layout. The first wiring model includes a wiring direction that is not available on any layer of at least one other wiring model in the set of wiring models. The method partitions the IC-layout region into several sub-regions. For each particular net, the method identifies the set of sub-regions containing the circuit elements of the particular net. For each particular net, the method retrieves a pre-computed attribute of a connection graph that is based on the first wiring model, and that represents the topology of interconnect lines needed to connect the identified set of sub-regions of the particular net. The method computes a placement cost for the IC layout within the region by using the retrieved attributes.

Applicants respectfully submit that Rostoker does not disclose, teach, or even suggest such a method. For instance, the Office Action cites column 58, line 36 to column 59, line 63 of Rostoker in support of the proposition that Rostoker discloses a method comprising selecting a first wiring model from among a plurality of wiring models, where each model specifying different types of interconnect lines. This portion of Rostoker describes an algorithm to reduce multi-pin nets into pairs of pins. However, this portion of Rostoker does not disclose selecting a first wiring model from a set of at least two wiring models, wherein each wiring model provides a wiring direction for each layer of the IC layout. Moreover, none of the portions cited in Rostoker

disclose, teach, or even suggest that the first wiring model includes a wiring direction that is not available on any layer of at least one other wiring model in the set of wiring models. Thus, Applicants respectfully submit that Rostoker does not disclose, teach, or even suggest several limitations of claim 42.

Accordingly, Applicants respectfully submit that Rostoker neither anticipates, nor otherwise invalidates claim 42. Since claims 43-45 are dependent on claim 42, Applicants respectfully submit that Rostoker neither anticipates, nor otherwise invalidates, claims 43-45 for at least the reasons discussed above in relation to claim 42.

In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(b) rejection of claims 42-45.

VII. Rejection of claims 38-41 under §102(e)

The Examiner rejected claims 38-41 under §102(e) as being anticipated by Kanazawa. Claims 39-41 are dependent on claim 38. Claim 38 is recited above. Applicants respectfully submit that Kanazawa does not disclose, teach, or even suggest the method of claim 38. For instance, the Office Action cites column 14, lines 40-44 of Kanazawa in support of the proposition that Kanazawa discloses a method comprising selecting a first wiring model from among a plurality of wiring models, where each model specifying different types of interconnect lines. This portion of Kanazawa lists techniques for wiring processing during global routing. Kanazawa specifically lists grid graph, checker board, and channel intersection graph models. However, this portion of Kanazawa does not disclose selecting a first wiring model from a set of at least two wiring models, wherein each wiring model provides a wiring direction for each layer of the IC layout. Moreover, none of the portions cited in Kanazawa disclose, teach, or even suggest that the first wiring model includes a wiring direction that is not available on any layer of

at least one other wiring model in the set of wiring models. Thus, Applicants respectfully submit that Kanazawa does not disclose, teach, or even suggest several limitations of claim 38.

Accordingly, Applicants respectfully submit that Kanazawa neither anticipates, nor otherwise invalidates claim 38. Since claims 39-41 are dependent on claim 38, Applicants respectfully submit that Kanazawa neither anticipates, nor otherwise invalidates, claims 39-41 for at least the reasons discussed above in relation to claim 38.

In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(e) rejection of claims 38-41.

VII. Rejection of claims 42-43 under §102(e)

The Examiner also rejected claims 42-43 under §102(e) as being anticipated by Kanazawa. Claim 43 is dependent on claim 42. Claim 42 is recited above.

Applicants respectfully submit that Kanazawa does not disclose, teach, or even suggest the method of claim 42. For instance the Office Action cites column 14, lines 40-44 of Kanazawa in support of the proposition that Kanazawa discloses a method comprising selecting a first wiring model from among a plurality of wiring models, where each model specifying different types of interconnect lines. This portion of Kanazawa lists techniques for wiring processing during global routing. Kanazawa specifically lists the grid graph, checker board, and channel intersection graph models. However, this portion of Kanazawa does not disclose selecting a first wiring model from a set of at least two wiring models, wherein each wiring model provides a wiring direction for each layer of the IC layout. Moreover, none of the portions cited in Kanazawa disclose, teach, or even suggest that the first wiring model includes a wiring direction that is not available on any layer of at least one other wiring model in the set of wiring models.

Thus, Applicants respectfully submit that Kanazawa does not disclose, teach, or even suggest several limitations of claim 42.

Accordingly, Applicants respectfully submit that Kanazawa neither anticipates, nor otherwise invalidates claim 42. Since claim 43 is dependent on claim 42, Applicants respectfully submit that Kanazawa neither anticipates, nor otherwise invalidates, claim 43 for at least the reasons discussed above in relation to claim 42.

In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the §102(e) rejection of claims 42-43.

CONCLUSION

In view of the foregoing, it is submitted that all claims, namely claims 28-45, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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